CLAIMS

1. A memory circuit, comprising:

a single polysilicon EEPROM cell having an erase margin voltage of above 0 V; and

an output node connected to said EEPROM cell capable of determining said erase margin voltage.

2. The circuit of claim 1, wherein said EEPROM cell comprises:

a semiconductor substrate having a surface;

a programming memory diffusion region in the semiconductor substrate;

a tunnel window formed by a tunnel oxide on said substrate surface overlying at least a portion of said memory diffusion;

a control gate memory diffusion region in the semiconductor substrate;

a dielectric interposed between the control gate and a floating gate structure;

said floating gate structure,

overlying at least a portion of the tunnel window,

forming the gate of a read transistor for said cell, and

overlying at least a portion of the control gate memory diffusion and capacitively coupled thereto; and

wherein said gate of said read transistor has a threshold voltage such that the erase margin voltage of said cell is above 0 V.

3. The circuit of claim 2, wherein said threshold voltage is achieved by manipulating at least one parameter in the process used to form said cell selected from channel dopant concentration, gate oxide thickness, dopant concentration in the floating and/or control gates, composition of the gate oxide, thickness and composition of the control gate capacitor dielectric, and coupling ratio between the floating gate and the control gate.

4. The circuit of claim 3, wherein said channel dopant concentration is about 1e15 to 5e17 cm^{-3} of boron, the gate oxide thickness is about 120 to 180 Å, the dopant concentration in the floating gate is about 5e19 to 5e20 cm^{-3} of phosphorus, the dopant concentration in the control gate is about 1e19 to 1e20 cm^{-2} of phosphorus and arsenic, the gate oxide comprises SiO_2, the control gate capacitor dielectric is about 125 to 200 Å thick and is composed of SiO_2, and the coupling ratio between the floating gate and the control gate is about 0.6 to 0.8.

5. The circuit of claim 4, wherein said channel dopant concentration is about 1e16 to 1e17 cm^{-3} of boron, the gate oxide thickness is about 155 Å, the dopant concentration in the floating gate is about 5e19 to 5e20 cm^{-3} of phosphorus, the dopant concentration in the control gate is about 1e19 to 1e20 cm^{-3} of phosphorus and arsenic, the gate oxide comprises SiO_2, the control gate capacitor dielectric is about 180 Å thick and is composed of SiO_2, the coupling ratio between the floating gate and the control gate is about 0.7.

6. The circuit of claim 2, wherein said threshold voltage is achieved with a read transistor gate no more than 4.5 times wide as it is long.

7. The circuit of claim 6, wherein the length of the floating gate is 0.5 μ and the width of the floating gate is about 2.0 μ.

8. The circuit of claim 7, wherein the read transistor gate has a threshold voltage of about 0.8 V.

9. The circuit of claim 1, wherein said output node comprises a drain line.

10. The circuit of claim 9, wherein said output node further comprises a sense amplifier connected to said EEPROM cell by the drain line and a source line, said sense amplifier capable of detecting margin voltages for said EEPROM cell.

11. The circuit of claim 1, wherein said EEPROM cell is a single row line EEPROM cell.

12. The circuit of claim 1, wherein said EEPROM cell is a dual row line EEPROM cell.

13. The circuit of claim 12, wherein said EEPROM cell is designed so that a field across said cell's tunnel window when biased is about 1.1 MV/cm.

14. A memory circuit, comprising:

a single polysilicon EEPROM cell having a drain line;

a margin test mode pull-up source device connected to said drain line, said margin test mode pull-up source device capable of producing an erase margin voltage of above 0 V in said EEPROM cell;

a sensor connected to said drain line capable of determining said erase margin voltage.

15. A memory circuit, comprising:

a single polysilicon EEPROM cell having a source line and a drain line;

a voltage control device connected to said source line, said voltage control device capable of producing an erase margin voltage of above 0 V in said EEPROM cell;

a sensor connected to said drain line capable of determining said erase margin voltage.

16. A method for evaluating an erase margin voltage in a single polysilicon EEPROM cell, said method comprising:

providing a memory circuit, comprising

an EEPROM cell having a control gate and an output node;

sweeping a voltage applied to said control gate through a range of voltages above about 0 V; and

determining from a signal on said output node when the margin voltage has been reached.

17. The method of claim 16, wherein said voltage is swept upward from about 0 V.

18. The method of claim 16, wherein said output node comprises a drain line.

19. The method of claim 16, wherein said output node further comprises a sense amplifier connected to said EEPROM cell by the drain line and a source line, said sense amplifier capable of detecting margin voltages for said EEPROM cell.

20. A memory circuit, comprising:

a single polysilicon EEPROM cell having a substrate and a backbiased control gate diffusion implant in said substrate, said cell having an erase margin voltage such that the backbiasing of said implant to said substrate is maintained; and

an output node connected to said EEPROM cell capable of determining said erase margin voltage.